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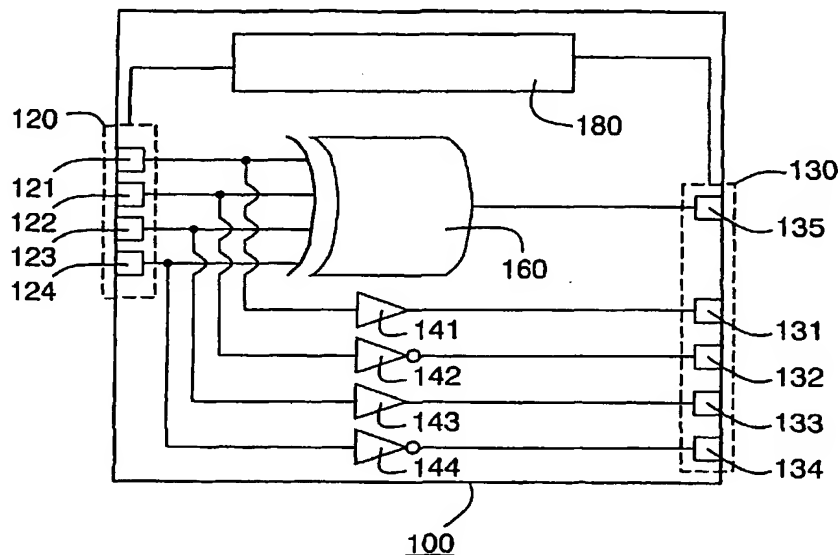
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— as to applicant's entitlement to apply for and be granted
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AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA,
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[Continued on next page]

(54) Title: ELECTRONIC CIRCUIT WITH TEST UNIT



(57) Abstract: A test arrangement for testing the interconnections of an electronic circuit (100) and a further electronic circuit is provided. A first selection of I/O nodes (120), which are arranged to receive input data in a functional mode of the electronic circuit (100), and which are coupled to a test unit in a test mode of the electronic circuit (100). The test unit has a combinational circuit (160) for implementing a multiple-input XOR or XNOR gate. The test unit also provides interconnections between the first selection of I/O nodes (120) and a second selection of I/O nodes (130) via logic gates (141-144). These interconnections increase the interconnect test coverage of the electronic device (100), because the interconnects with the further electronic circuits that are associated with I/O nodes (131-134) become testable as well.

**Declaration under Rule 4.17:**

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B. FIELDS SEARCHED

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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 99 39218 A (MURIS MATHIAS N M ; RAAYMAKERS ROBERTUS M W (NL); JONG FRANCISCUS G) 5 August 1999 (1999-08-05) page 12 -page 16; figures 1,3,4 & EP 0 979 418 A (KONINKL PHILIPS ELECTRONICS NV) 16 February 2000 (2000-02-16) cited in the application --- -/--	1, 2, 4-8

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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